Patent

Customer No.: 31561
Docket No. 9945-US-PA-1
Application No.: 10/707,874

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Applicant	: Kent Kuohua Chang
Application No.	: 10/707,874
Filed	: January 20, 2004
For	: METHOD OF FABRICATING MULTI-BIT FLASH MEMORY
Art Unit	: 2823
Examiner	: TOLEDO, FERNANDO L.

TRANSMITTAL LETTER
002-1-571-273-8300
(Via Courier: 1+6 pages)

Assistant Commissioner for Patents
Alexandria, VA 22314

Dear Sir,

In response to the Notice of Non-Compliant Amendment dated August 29, 2005, please find the Supplementary Amendment in 6 pages.

I believe that no fee is incurred. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.:9945-US-PA-1).

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: September 2, 2005 By: Belinda Lee
Belinda Lee
Registration No.: 46,863

Please send future correspondence to:
7F.-1, No. 100, Roosevelt Rd.,
Sec. 2, Taipei 100, Taiwan, R.O.C.
Tel: 886-2-2369 2800 Fax: 886-2-2369 7233 / 886-2-2369 7234
E-MAIL: BELINDA@JCIPGroup.com.tw; USA@JCIPGroup.com.tw

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Application No.: 10/707,874
Docket No.: 9945-US-PA-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: Toledo, Fernando L

Group Art Unit: 2823

In re PATENT APPLICATION of
Applicants : Kent Kuohua Chang

Serial No. : 10/707,874

Filed : January 20, 2004

For : Method Of Fabricating Multi-Bit Flash Memory

AMENDMENT

Attorney Docket: 9945-US-PA-1

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.: 9945-US-PA-1)

SUPPLEMENTARY AMENDMENTS TO NON-FINAL OFFICE ACTION

United States Patent and Trademark Office
Customer Service Window, Mail Stop **Amendment**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In reply to the Notice of Non-Compliant Amendment dated August 29, 2005, Applicant respectfully submits the following Amendments.

Customer No.: 31561
Application No.: 10/707,874
Docket No.: 9945-US-PA-1

AMENDMENT

Please amend claims as follows.

In the Claims :

Claims 1-7. (cancelled)

8. (currently amended) A method of fabricating a multi-bit flash memory, comprising:

providing a substrate;

forming a tunneling oxide layer on the substrate;

forming a conductive layer on the tunneling oxide layer;

forming an isolation layer in the conductive layer to partition the conductive layer into ~~a plurality of~~ more than two conductive blocks arranged in an array with a plurality of rows extending from a region predetermined for forming one bit line to another region predetermined for forming another bit line and a plurality of columns, wherein each row comprises two conductive blocks, and each column comprises ~~n (n is a positive integer)~~ more than two conductive blocks;

forming a gate dielectric layer on the conductive layer;

patterning the gate dielectric layer and the conductive layer to form a floating gate;

forming the bit lines in the substrate at two sides of the floating gate;

forming a control gate on the floating gate; and

performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows.

9. (original) The method according to Claim 8, wherein the material of the

conductive layer comprises germanium polycide.

10. (original) The method according to Claim 8, wherein the step of forming the isolation region further comprises:

forming a patterned photoresist layer on the conductive layer to expose a part of the conductive layer predetermined for forming the isolation region;

performing an ion implantation step to implant dopant into the exposed conductive layer; and

performing an annealing process to react the dopant with silicon of the conductive layer to form the isolation region.

11. (original) The method according to Claim 10, wherein the dopant includes oxygen ions.

12. (original) The method according to Claim 11, wherein ion implantation step is performed with a dosage of dopant of about 1×10^{18} atoms/cm^2 to about 2×10^{18} atoms/cm^2.

13. (original) The method according to Claim 11, wherein the ion implantation step is performed with an implantation energy of about 20 KeV to about 80 KeV.

14. (original) The method according to Claim 10, wherein the dopant includes nitrogen ions.

15. (original) The method according to Claim 10, wherein the annealing process is performed at about 950°C to about 1150°C.

16. (original) The method according to Claim 8, further comprising a step of forming a field oxide layer after the step of forming the bit lines and before the step of forming the control gate.